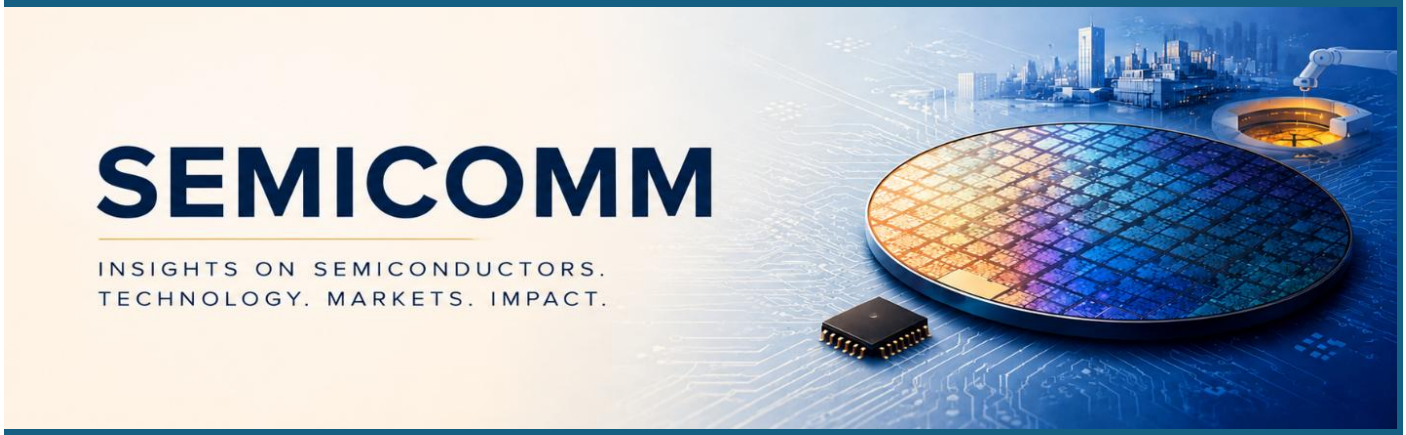
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The Semiconductor Fab Handbook

A Bottom-Up Guide to Building, Operating, and Profiting From a 28nm/45nm Semiconductor Fab

The Semiconductor Fab Handbook



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White paper for new semiconductor manufacturers, investors, materials suppliers, and ecosystem planners

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Executive Summary

Semiconductors have become one of the world's most strategically important industries, underpinning artificial intelligence, cloud computing, automotive electronics, industrial automation, communications infrastructure, and consumer devices. As governments and corporations invest billions of dollars into new manufacturing capacity, a fundamental question remains:

What does it take to build and operate a successful semiconductor fabrication facility?

Building a semiconductor fab is not simply a construction project. It is a long-cycle manufacturing capability project that combines process technology, equipment, materials, utilities, workforce development, yield learning, customer qualification, supply-chain resilience, and financial discipline.

For a new manufacturer, the central question is not only whether a fab can be built, but whether it can reach:

- Stable yield
- Qualified customers
- High utilization
- Reliable utilities
- Controlled materials
- Competitive wafer cost
- Sustainable profitability

A full-scale 300mm mature-node fab operating at 40,000-50,000 wafer starts per month (WSPM) requires significant capital, technology access, operational expertise, and customer demand. As a public benchmark, Tata Electronics' Dholera 300mm fab has been described as a 50,000 wafers-per-month facility spanning 28nm to 110nm technologies, with an announced investment of approximately US$11 billion.[1-3]

For most new entrants, a pure 28nm-first strategy is rarely the optimal path. A more realistic approach is to establish a 300mm **mature-node** platform, initially ramping more mature (90-45nm technologies before introducing 28nm. This progression allows the manufacturer to build stable process control, low defectivity, customer-qualified process design kits (PDKs), reliable utility infrastructure, and predictable yield performance.[4]

This white paper examines what it takes to build and operate a semiconductor manufacturing fab from the ground up. Through a structured end-to-end assessment (using a representative base case as below), we analyze the technology, infrastructure, equipment, materials, utilities, workforce, yield, supply-chain, customer, and financial requirements needed to transform a greenfield fab investment into a sustainable and profitable semiconductor manufacturing business.

Representative Base-Case Fab used for this study:

Reasons for these assumptions are explained in the next sections.

Metric	Base-Case Assumption
Wafer size	300mm
Installed capacity	40,000 WSPM
Target utilization	85%
Effective wafers/year	408,000 wafers
Technology path	45/40nm ramp → 28nm expansion
Cleanroom area	20,000-40,000 m^2
Employees	~2,500-3,000
CAPEX range	US$7B-10B (planning estimate)
Revenue potential	~US$1.0B/year at US$2,500/wafer
Yield target	>85% mature functional yield
Tool availability target	>90% for critical tools

Key takeaway:

A fab becomes successful only when the building, tools, process, materials, people, customers, and economics all work together. A cleanroom without qualified customers is a depreciation machine. A process without yield is not a business. A 28nm fab without high utilization is financially fragile.

1. The Technology-Market Decision

The first decision is not technical; it is commercial. Before selecting a process technology, a new manufacturer must determine which node offers the optimal balance between market demand, manufacturing complexity, capital intensity, customer requirements, and long-term competitive differentiation.

This section evaluates the relative attractiveness of key semiconductor nodes and identifies the factors that influence node selection for a new fab entrant, including process complexity, capital expenditure requirements, ecosystem maturity, customer demand, and long-term market potential.

1.1 Technology Node comparison

When discussing semiconductor manufacturing, attention is often focused on leading-edge technologies such as 3nm, 2nm, and future process nodes. However, the majority of semiconductor volume continues to be produced on mature and mid-mature technologies. Automotive electronics, industrial automation, communication infrastructure, consumer devices, display controllers, power management ICs, and many IoT products do not require the most advanced transistor geometries to remain competitive.

Node	Typical applications	Complexity	Capex	Market attractiveness
180nm	Automotive, industrial, analog, power	Low	Low	Mature
130nm	Microcontroller unit (MCU), analog, automotive	Low-medium	Low	Mature
90nm	MCU, connectivity, industrial	Medium	Medium	Mature
65nm	MCU, connectivity, display, embedded logic	Medium	Medium	Strong
45/40nm	MCU, automotive, connectivity, display, mixed-signal	Medium-High	High	Strong
28nm	Connectivity, display, automotive logic, edge AI, consumer SoC	High	High	Very strong
22nm FD-SOI	Automotive, IoT, RF, low-power logic	High	High	Niche/specialty

For a new semiconductor manufacturer, the critical question is therefore not: "What is the most advanced node available?" but rather: **"Which node provides the best balance between market demand, manufacturing complexity, capital investment, and long-term profitability?"**

Among mature and mid-mature technologies, **28nm** has emerged as one of the industry's most commercially successful process nodes, often referred to as the industry's "golden node", the reasons for which are discussed in the next section.

1.2 Why 28nm Became a Strategic "Golden Node"

28nm technology node occupies an unusual position in semiconductor manufacturing, as it is in between traditional mature technologies and advanced nodes. This node provides substantial improvements in transistor density, power efficiency, and integration capability while avoiding the extreme complexity and cost associated with FinFET and EUV-based manufacturing.[5]

The commercial success of 28nm can largely be attributed to six structural advantages:

- Strong balance between performance and manufacturing cost
- Broad applicability across multiple end markets
- Long commercial lifecycle
- Attractive return on invested capital
- Large and mature design ecosystem
- Extensive global manufacturing infrastructure

Unlike older mature nodes, 28nm delivers sufficient performance for complex digital, connectivity, display, and automotive applications. At the same time, it avoids many of the manufacturing challenges introduced by FinFET-based technologies.

Feature	28nm	20nm	16nm / 14nm and below
Transistor type	Mostly planar CMOS, often HKMG variants	Planar, more complex	FinFET
Lithography	DUV immersion / dry DUV	DUV multiple-patterning heavy	DUV + EUV or advanced multi-patterning
Manufacturing complexity	High but manageable	Higher	Very high
Design cost	High	Higher	Very high
Economic position	Strong mature-node sweet spot	Transitional	Advanced-node economics

From a manufacturing perspective, 28nm is particularly attractive because it remains a predominantly planar CMOS technology, allowing fabs to leverage mature **DUV lithography** infrastructure while achieving significantly higher integration levels than 45nm or 65nm processes.

1.3 Why choose even more mature nodes (e.g. 45/40nm) as a new manufacturer?

Advantages of 28nm

A manufacturer may choose 28nm because it offers:

- Higher transistor density
- Lower cost per function
- Better power-performance characteristics
- Smaller die size for complex designs
- Strong relevance for:
    - Connectivity ICs
    - Display controllers
    - Advanced MCUs
    - Edge AI processors
    - Consumer SoCs
    - Automotive control systems
- Higher potential wafer average selling price (ASP) compared with older mature nodes. Public estimates place 28nm 300mm wafer pricing around US$ 2,550 – US$ 3,450, with an average near US$ 3,000.[7]

The node continues to support high-volume production across consumer, industrial, networking, and automotive markets while remaining accessible to DUV-based manufacturing.

Advantages of 45/40nm

However, a new manufacturer may instead prioritize 45/40nm because it provides:

- Lower process complexity.
- Faster yield learning.
- Lower defect sensitivity.
- Simpler lithography requirements.
- Lower customer qualification risk.
- Strong automotive and industrial adoption.
- Good wafer ASP in the estimated range of US$1,800 – 2,500 per 300mm wafer.

For a first-time fab operator, these factors can significantly reduce execution risk during the early years of operation.

Strategic Recommendation

For most new semiconductor manufacturers, the optimal strategy is not to begin with high-volume 28nm production immediately. A more practical roadmap is:

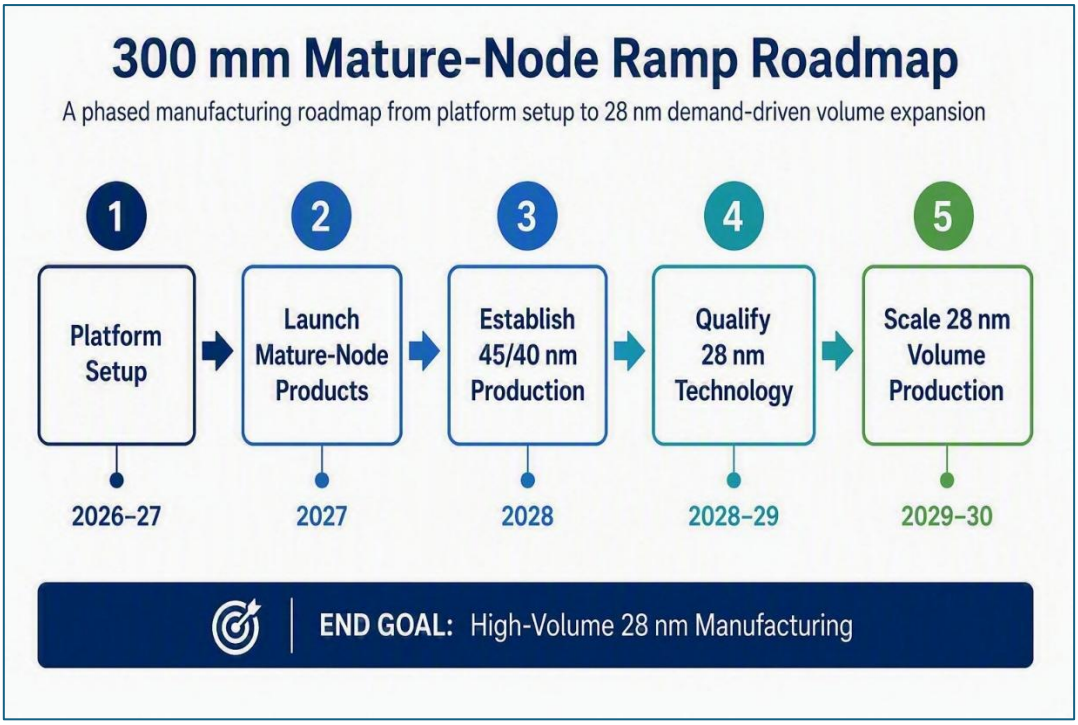


Figure 1: Simplified roadmap illustrating the phased evolution of a 300 mm fab from platform setup to high-volume 28 nm manufacturing.

This phased progression allows the organization to build the following capabilities before introducing the additional complexity associated with large-scale 28nm production:

- Process integration expertise.
- Yield-management capability.
- Metrology and inspection discipline.
- Manufacturing culture.
- Customer confidence.
- Supply-chain maturity.

Key takeaway:

Mature nodes remain the foundation of modern semiconductor manufacturing. Among them, 28nm represents one of the best balances ever achieved between performance, manufacturing complexity, ecosystem maturity, capital efficiency, and market demand, making it a highly attractive destination for new semiconductor manufacturers. However, a new manufacturer should usually build a 45/40nm-capable platform first and use it as the operational bridge to 28nm.

2. The Hypothetical Fab Definition

Before evaluating equipment, materials, workforce, or financial performance, the manufacturing strategy must be clearly defined. The selected technology node, capacity, product mix, and business model determine virtually every aspect of fab design, including:

- Cleanroom size
- Equipment requirements
- Utility demand
- Workforce requirements
- Process complexity
- Supply-chain requirements
- Capital expenditure
- Customer qualification requirements

For this white paper, a representative mature-node foundry is modelled to evaluate the technical and economic feasibility of a new semiconductor manufacturing operation.

***Important**: This is an analytical base case. Actual cost and ramp timing depend heavily on country, subsidies, labour cost, utility reliability, local ecosystem, equipment availability, technology partner, process complexity, and construction strategy.*

2.1 Base-case fab specification

Commercial Definition

Parameter	Base-Case Assumption
Fab Type	Greenfield 300mm Foundry
Business Model	Pure-play foundry
Technology Platform	45/40nm initial production, 28nm expansion
Wafer Size	300mm
Installed Capacity	40,000 WSPM
Utilization Target	85-90%
Ramp Period	5 years
Primary Markets	Automotive, Industrial, Connectivity, Display, MCU, Edge Computing
Packaging Strategy	External OSAT during initial ramp
Technology Source	Licensed platform or technology-transfer partner

Technology Platform Assumptions (45/40nm Initial Production with 28nm Expansion)

Parameter	Base-Case Assumption
Technology Platform	45/40nm initial production, expandable to 28nm
Transistor Architecture	Planar CMOS
Gate Stack	Poly-Si gate for 45/40nm; High-K Metal Gate (HKMG) for 28nm
Isolation Scheme	Shallow Trench Isolation (STI)
Source/Drain Formation	Ion implantation with advanced anneal integration
FEOL Complexity	High (45/40nm), Very High (28nm)
FEOL Process Steps	~200-300 (45/40nm), ~250-350 (28nm)
FEOL Mask Layers	~15-20 (45/40nm), ~18-25 (28nm)
Critical FEOL Lithography Layers	~8-12 (45/40nm), ~12-18 (28nm)
MOL Complexity	Contact and local interconnect formation
MOL Process Share	~10-15% of total process flow
BEOL Metal Layers	8-10 (45/40nm), 10-12 (28nm)
BEOL Process Share	~35-45% of total process flow
Lithography Platform	ArF Immersion (193nm), ArF Dry (193nm), KrF (248nm)
Lithography Burden	High (45/40nm), Very High (28nm)
Metrology Burden	High (45/40nm), Very High (28nm)
Total Mask Count	~35-45 (45/40nm), ~40-55 (28nm)
Total Process Steps	~450-650 (45/40nm), ~600-800 (28nm)
Fabrication Cycle Time	~50-80 days (45/40nm), ~60-90 days (28nm)
Design Enablement	Standard-cell libraries, SRAM compilers, I/O libraries
Process Design Kit (PDK)	Full customer-qualified PDK
Reliability Capability	Automotive and industrial qualification support
Defect Density Target	<0.1 defects/cm^2 at mature production
Target Functional Yield	85-95% at mature production
Process Integration Difficulty	High (45/40nm), Very High (28nm)
Technology Source	Licensed platform, JV partner, or technology-transfer partner

Physical Scale Assumptions

Parameter	Planning Value
Total site area	100-250 acres
Fab building area	40,000-80,000 m^2
Cleanroom area	20,000-40,000 m^2
Utility area	15,000-30,000 m^2
Warehouse area	5,000-15,000 m^2
Office/support area	5,000-10,000 m^2

Process Complexity Assumptions (Compiled)

Metric	45/40nm	28nm
FEOL Masks	15-20	18-25
MOL Masks	2-5	3-5
BEOL Masks	20-25	22-30
Total Masks	35-45	40-55
FEOL Steps	200-300	250-350
MOL Steps	50-80	70-100
BEOL Steps	200-270	280-350
Total Steps	450-650	600-800
Critical Lithography Layers	15-20	20-30
Fabrication Cycle Time	50-80 days	60-90 days
Lithography Burden	High	Very High
Metrology Burden	High	Very High
Process Integration Difficulty	High	Very High

Important: These are planning-level assumptions. Actual numbers depend on process architecture, product type, foundry platform, reliability options, and customer requirements.

Why This Configuration?

This configuration was selected because it represents the most realistic entry point for a new foundry operator:

- Large enough to achieve manufacturing scale
- Mature enough to reduce technology risk

- Advanced enough to attract connectivity, automotive, and display customers
- Does not require EUV infrastructure
- Supports long-term expansion into higher-value nodes

2.2 Manufacturing Targets

A fab should not be defined only by wafer starts. It should be defined by the products it intends to manufacture.

Target Product Portfolio

Product Type	Typical Process Node
Automotive MCU	40nm - 90nm
Industrial MCU	40nm - 130nm
Connectivity IC	28nm - 65nm
Display Driver IC	28nm - 55nm
Network Processor	28nm - 45nm
Edge AI Controller	28nm
Industrial SoC	28nm - 45nm
Security Controller	40nm - 90nm

Typical Die Characteristics

Metric	Assumption
Average Die Size	50-150 mm^2
Gross Dies / 300mm Wafer	~400-1300
Functional Yield Target	85-95%
Wafer Sort Yield	95-99%
Packaging Yield	98-99.5%
Final Test Yield	95-99%

These values are illustrative and product dependent.

A 50mm^2 die and a 150mm^2 die processed on the same node can have dramatically different economics because gross die count and defect sensitivity change with die area.

These assumptions will later drive:

- Revenue
- Material consumption
- Yield
- Cost per good die
- Packaging requirements
- Customer economics

2.3 Required site elements

A 40,000 WSPM 300mm fab requires more than a cleanroom. The manufacturer must plan for:

- Land
- Fab building
- Cleanroom
- Sub-fab
- Office and support buildings
- Utility buildings
- Chemical storage and distribution
- Specialty gas farms
- Bulk gas systems
- Wastewater treatment
- Electrical substation
- UPW plant
- Chillers
- HVAC systems
- Exhaust and abatement
- Warehouse
- Logistics docks
- Maintenance shops
- Training center
- Emergency response infrastructure
- EHS infrastructure
- Security infrastructure
- Data and manufacturing-control infrastructure

Representative FAB value-creation process flow:



Figure 2: Semiconductor fab value-creation flow, illustrating the progression from site and infrastructure readiness to qualified products, customers, and cash generation.

3. Fab Architecture and Process Flow

A fab converts incoming silicon (Si) wafers into finished wafers through repeated cycles of patterning, material addition, material removal, doping, planarization, cleaning, and measurement. Semiconductor fabrication involves many sequential process steps, including lithography, deposition, etch, implant, diffusion/anneal, CMP, cleaning, metrology, wafer sort, assembly, packaging, and testing.[9]

3.1 High-level process flow



Figure 3: High-level 300 mm semiconductor manufacturing flow from wafer input to customer-qualified mass production.

3.2 FEOL, MEOL, and BEOL split

Module	Purpose	Approximate Process Share
FEOL	Transistor formation	40-50%
MOL	Contact and local interconnect	10-15%
BEOL	Metal interconnect and passivation	35-45%

3.3 Major process modules

Module	Typical Equipment	Key Materials	Major Yield Risk	Cost Driver
Lithography	Scanner, coat/develop track	Resist, BARC, developer, solvents	CD variation, overlay, defects	Scanner/track utilization
Etch	Plasma etcher	CF_4, Cl_2, HBr, O_2, C_4F_8	Residue, profile control, selectivity	Chamber productivity
Deposition	CVD, ALD, PVD	Precursors, targets	Film defects, thickness variation	Tool throughput, precursor consumption
Implant	Ion implanter	Dopant sources/gases	Dose/energy variation, Vt variation	Implant utilization
Thermal	RTP, furnace	N_2, O_2, process gases	Activation issues, thermal excursions	Thermal budget / throughput
CMP	CMP polisher, post-CMP clean	Slurry, pads, conditioners	Scratches, dishing, erosion	Consumables + throughput
Cleans	Wet bench, single-wafer clean	HF, HCl, NH_4OH, H_2O_2, UPW	Particles, metallic contamination	Chemical + UPW consumption
Metrology	CD-SEM, OCD, film/overlay tools	Reference wafers, calibration standards	Measurement drift, tool matching	Sampling rate / throughput
Inspection	Optical inspection, e-beam review	Inspection recipes, calibration wafers	Defect escape, detection sensitivity	Throughput / sampling intensity

For every module, a fab manufacturer must define:

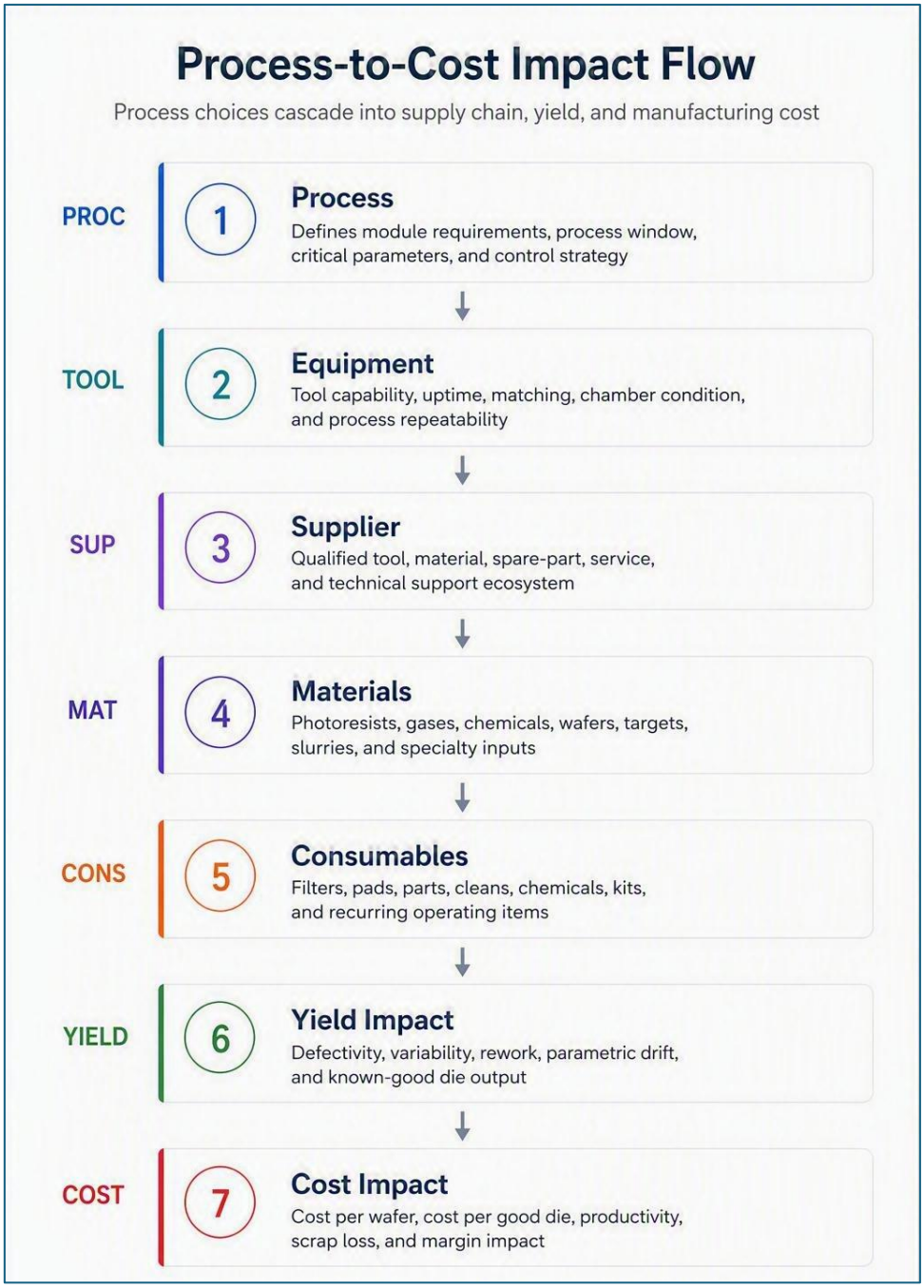


Figure 4: Process-to-cost impact flow showing how semiconductor process requirements cascade through equipment, suppliers, materials, and consumables to influence yield and total manufacturing cost.

4. Equipment bill of materials (BOM)

The equipment BOM is one of the most important components of fab economics. Knowing that a fab requires lithography, etch, deposition and CMP tools is not enough. The business case depends on:

- Tool count
- Throughput
- Availability
- Bottleneck capacity
- Utilization
- Maintenance
- Chamber configuration
- Redundancy
- Qualification requirements
- Spare-parts availability
- Tool lifetime

The correct calculation is:

Process flow → process steps → throughput requirement → tool capacity → tool count

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4.1 Main equipment categories

Module	Key tools	Typical suppliers
Lithography	ArF immersion scanner, ArF dry scanner, KrF scanner, coat/develop track	ASML, Nikon, Canon, TEL, SCREEN
Etch	Dielectric etch, conductor etch, spacer etch, hard-mask etch, strip	Lam Research, TEL, Applied Materials
Deposition	CVD, PECVD, ALD, PVD, epitaxy	Applied Materials, Lam Research, TEL, ASM
Implant	High-current, medium-current, high-energy implanters	Applied Materials, Axcelis
Thermal	Rapid Thermal Processing (RTP), furnace, spike anneal	TEL, Applied Materials, Kokusai
CMP	Polishers, post-CMP clean, slurry delivery	Applied Materials, Ebara, Lam Research
Cleans	Wet benches, single wafer cleans, megasonic cleans	SCREEN, TEL, Lam Research
Metrology	CD-SEM, overlay, films, OCD, X-ray metrology	KLA, Applied Materials, Onto, Nova

Inspection	Optical inspection, e-beam review, wafer inspection	KLA, Applied Materials, Onto
Automation	AMHS, FOUP handling, MES, APC, FDC	Daifuku, Murata, Siemens, Applied Materials, PDF Solutions

DUV lithography systems – including ArF immersion, ArF dry and KrF systems – remain important for mature and mid-mature semiconductor manufacturing where EUV is not required.

4.2 Indicative Equipment CAPEX Split

Module	Typical Share of Equipment Budget
Lithography	25-35%
Etch	15-20%
Deposition	15-20%
CMP	5-10%
Implant	5-10%
Metrology and inspection	10-15%
Automation	2-5%

Global 300mm fab equipment spending is projected by SEMI to reach US$133B in 2026, US$151B in 2027, US$155B in 2028, and US$172B in 2029, showing the scale of global equipment investment.[6]

4.3 Indicative tool-count logic

A full 40,000-WSPM fab requires sufficient tool capacity to prevent manufacturing bottlenecks. Exact counts depend on:

- Number of process steps
- Number of critical layers
- Wafer cycle time
- Tool throughput
- Tool availability
- Preventive maintenance
- Product mix
- Process duplication
- Chamber configuration
- Redundancy strategy
- Ramp requirements

Module	Tool-count logic	Indicative tools for 40k WSPM	Short reason for estimate
Lithography	Critical-layer count, scanner throughput, track capacity and utilization	25–35 scanners + 15–20 tracks	40/45 nm uses multiple DUV tool classes; high scanner throughput means fewer systems are needed than the number of lithography layers might suggest.
Etch	Etch steps per wafer, chamber productivity and recipe mix	35–50 systems	Many etch steps, but multi-chamber platforms provide high parallel capacity.
Deposition	Film-stack complexity and batch/single-wafer requirements	30–45 systems	Multiple CVD, PVD, ALD and other deposition applications require dedicated capacity.
CMP	Planarization levels, throughput and post-CMP cleaning	15–25 systems	Relatively few CMP steps and high tool throughput, with some material-specific duplication.
Implant	Implant steps, dose/energy requirements and throughput	10–18 systems	High throughput but several energy/current regimes require separate capacity.
Thermal / RTP / Furnace	Anneal, oxidation, diffusion and activation steps	25–40 systems	Numerous thermal steps, with batch furnaces providing high wafer capacity.
Wet Clean / Strip	Cleaning frequency, strip steps and throughput	15–25 systems	Cleaning occurs repeatedly throughout the flow and requires several dedicated process types.
Metrology	Sampling rate, control plan and measurement time	35–55 systems	Many measurements are required, but only a controlled sample of wafers/layers is typically measured.
Inspection	Defect-learning intensity, inspection frequency and quality requirements	10–20 systems	Inspection is concentrated on critical layers and process-control points rather than every wafer/step.

Important: *A new entrant should not minimize metrology and inspection simply to reduce initial CAPEX. During ramp, these systems are essential for:*

- *Defect identification*
- *Root-cause analysis*
- *Process-window development*
- *Excursion detection*
- *Yield learning*
- *Customer qualification*

Underinvestment can therefore reduce CAPEX while increasing the time required to achieve stable yield.

5. Materials BOM

A fab is a high-purity materials consumption engine. For a 28nm/45nm fab, materials are not simply operating inputs. Their following properties can directly affect process capability, yield and reliability:

- Purity
- Particle performance
- Metal contamination
- Chemical stability
- Lot-to-lot consistency
- Shelf life
- Packaging
- Supply reliability

5.1 Main Materials Categories

Module	Key Materials
Lithography	ArF immersion resist, ArF dry resist, KrF resist, BARC, SOC, topcoat, developer, rinse, EBR, solvents
Etch	CF_4, CHF_3, C_4F_8, SF_6, Cl_2, HBr, O_2, Ar, He, chamber clean gases
Deposition	SiH_4, TEOS, NH_3, N_2O, WF_6, Cu/Al/Ti/Ta targets, high-k precursors
CMP	Oxide slurry, tungsten slurry, copper slurry, barrier slurry, pads, conditioners, post-CMP cleans
Cleaning	HF, H_2SO_4, H_2O_2, NH_4OH, HCl, IPA, TMAH, solvents, UPW

We can describe semiconductor fabrication as relying on gases, chemicals, solvents, ultrapure water, deposition precursors, ion implantation gases, cleaning chemistries, and repeated process control steps.[10]

5.2 Annual material cost model

The manufacturer should calculate material cost as follows:

$$Annual\ material\ cost = Material\ cost\ per\ processed\ wafer \times Annual\ processed\ wafer$$

$$Annual\ processed\ wafer = 40{,}000\ WSPM \times 12 \times 85\% = \mathbf{408{,}000\ wafers\ per\ year}$$

Assume mature-node material cost:

Scenario	Material Cost / Wafer	Annual Materials Cost
Conservative	US$700	US$286M
Base	US$900	US$367M
High	US$1,100	US$449M

5.3 Representative Materials Spend Split

Category	Share of Materials Spend	Base-Case Annual Spend at US$367M
Silicon wafers	15-25%	US$55M-92M
Lithography materials	15-20%	US$55M-73M
Wet chemicals	10-15%	US$37M-55M
Gases	10-15%	US$37M-55M
CMP materials	10-15%	US$37M-55M
Deposition precursors / targets	10-20%	US$37M-73M
Masks / Pellicles related	5-15%	US$18M-55M

The next layer should include:

- Safety stock
- Supplier lead time
- Dual-source availability
- Qualification time
- Geographic concentration
- Emergency supply capability
- Change-control requirements

Key manufacturing lesson: *Materials are not commodities at 28nm/45nm. Supplier quality, metal contamination, particle control, storage conditions, shelf life, lot-to-lot variation, and change-control discipline directly affect yield.*

6. Utilities: The Invisible Semiconductor Factory

A fab is almost as much a utilities and chemical infrastructure project as it is a semiconductor process project. The process equipment cannot operate without:

- Stable electricity
- HVAC
- Cooling
- UPW
- Bulk gases
- Specialty gases
- Exhaust
- Abatement
- Wastewater treatment

6.1 Electricity

Electricity demand comes from:

- Process tools
- Vacuum pumps
- Chillers
- HVAC
- Cleanroom air handling
- UPW production
- Exhaust
- Gas abatement
- Wastewater treatment
- Data systems and automation

Power requirements increase significantly as the fab progresses from construction to full production.

Phase	Power requirement
Construction	Low to medium
Tool installation	Medium
Initial operation	High
Full capacity	Very high

The electrical design should include:

- High-voltage supply
- Substations
- UPS systems

- Emergency generation
- Power-quality management
- Redundancy
- Expansion capacity

Power calculation

Assume average power draw:

Scenario	Average Power	Annual Electricity
Low	50 MW	438 GWh/year
Base	80 MW	701 GWh/year
High	150 MW	1,314 GWh/year

Calculation

$$Annual\ electricity = Average\ MW\ \times 8{,}760 \frac{hours}{year}$$

$$Base\ case: 80MW\ \times 8{,}760 = 701\ GWh/year$$

6.2 Water and UPW

Water must be separated into:

- Raw water
- Process water
- UPW
- Cooling water
- Recycled water
- Wastewater
- Discharge water

MKS states that UPW is used in surface cleaning, wet etch, solvent processing, and CMP, and that a 200mm fab processing 20,000 wafers/month can use up to 3,000 m^3/day of UPW. MKS also cites ITRS values of 7 liters/cm^2 of UPW per wafer out and a later target of 4.5 liters/cm^2.[12] Semiconductor Engineering also notes that fabs withdraw large volumes of water, though significant portions can be treated and reused, with cooling towers often representing a major loss path.[13]

Base case UPW Calculation

$$300mm\ wafer\ area\ =\ 706.9\ cm2$$

Daily wafer starts at 40,000 WSPM and 85% utilization:

$$Daily\ wafers = (40{,}000\ \times 85\%) \div 30 = 1{,}133\ wafers/day$$

Daily wafer surface area:

$$1{,}133 \times 706.9 cm^2 = 801{,}918 \ cm^2/day$$

UPW demand using 4.5-7 L/cm^2:

$$Low\ case: 801{,}918 \times 4.5L = 3{,}609 \ m^3/day$$

$$High\ case: 801{,}918 \times 7L = 5{,}613 \ m^3/day$$

Estimated UPW Demand

Scenario	UPW Demand
Low	~3,600 m^3/day
High	~5,600 m^3/day

6.3 Gas systems

Gas type	Examples	Infrastructure implication
Bulk gases	N_2, O_2, Ar, H_2, He	Bulk storage or on-site generation
Specialty gases	WF_6, SiH_4, NH_3, NF_3, CF_4, Cl_2, HBr	Gas cabinets, toxic gas monitoring, abatement
Safety-critical gases	Pyrophoric, corrosive, toxic gases	Redundant safety systems and EHS procedures

Gas infrastructure requires:

- Storage
- Distribution
- Gas cabinets
- Leak detection
- Toxic-gas monitoring
- Emergency shutoff
- Exhaust
- Abatement
- Redundancy

6.4 Waste streams

A mature-node fab must manage:

- Acid waste
- Solvent waste
- Slurry waste
- Fluorinated gases
- Heavy-metal waste

- Wastewater
- Contaminated filters
- Used containers
- Spent chemicals

Key message:

Utility failure can cause wafer scrap, tool downtime, safety events, customer delays, and yield excursions. Utilities are not background infrastructure; they are part of the manufacturing process.

7. People and Operating Model

A new fab needs experienced people before it needs volume. The most critical early hires are people who have already:

- Ramped a fab
- Transferred a process
- Qualified equipment
- Reduced defectivity
- Stabilized yield
- Managed excursions
- Qualified customers
- Built manufacturing organizations

A new fab can purchase equipment. It cannot purchase manufacturing culture overnight.

7.1 Estimated headcount for 40,000 WSPM fab

The following is an analytical estimate for a 300mm mature-node fab with moderate automation. Actual headcount can vary significantly with:

- Automation level
- Labor cost
- Outsourcing
- Site maturity
- Shift structure
- Product mix
- Facilities operating model

Function	Estimated employees	Share	Short reasoning
Manufacturing operations	700	26%	24/7 shift coverage for wafer handling, production monitoring, lot dispatch and manufacturing supervision.
Equipment engineering	450	16%	Supports equipment uptime, preventive maintenance, troubleshooting, qualification and tool improvement.
Process engineering	350	13%	Handles process control, optimization, SPC, recipe development and process excursions.
Yield and integration	220	8%	Drives yield improvement, defect reduction and integration across process modules.
Facilities and utilities	320	12%	Operates cleanroom, HVAC, UPW, gases, chemicals, electrical and waste infrastructure.

Quality and reliability	140	5%	Manages quality systems, reliability, audits, customer requirements and failure analysis.
IT, automation, MES, APC	140	5%	Supports MES, AMHS, FDC, APC, automation infrastructure and fab IT systems.
Supply chain and procurement	120	4%	Manages materials, chemicals, spare parts, logistics and supplier relationships.
Business and customer engineering	120	4%	Supports customer interface, product engineering, applications and technical programs.
Corporate, EHS, security	180	7%	Covers HR, finance, administration, EHS, security and site-level management.
Total	**2,740**	100%	Planning-level staffing estimate for a 40k-WSPM 300 mm mature-node fab.

These numbers should be used as planning assumptions, not as universal industry benchmarks.

Employees per 1,000 WSPM:

$$Employees\ per\ 1000\ WSPM = 2{,}740 \div 40 = \mathbf{68.5}$$

For mature node 300mm fab, 70-100 employees per 1000 wafers suggests a reasonable efficient, moderately automated 300mm foundry, which is a realistic assumption for a 45/40nm to 28nm manufacturing platform

7.2 Critical roles

- Fab general manager
- Technology-transfer leader
- Process integration leads
- Lithography experts
- Etch experts
- Deposition experts
- CMP experts
- Defect-reduction engineers
- Yield engineers
- Equipment maintenance leaders
- Facilities engineers
- PDK and design-enablement team
- Reliability and quality team
- Customer engineering team
- Supply-chain quality specialists
- Manufacturing IT and automation specialists

7.3 Operating model

A production fab requires:

- 24/7 shift structure
- Preventive maintenance
- Tool qualification discipline
- Statistical Process Control (SPC)
- Advanced Process Control (APC)
- Fault Detection and Control (FDC)
- Excursion management
- Lot genealogy
- Recipe management
- Process-change control
- Customer quality systems
- Supplier quality management
- Emergency response
- EHS procedures

> ***Key message:*** *Operators run lots, but engineers run the fab. Yield maturity depends on process integration, equipment stability, defect learning, and disciplined manufacturing culture.*

8. From Wafer to Customer

A fab does not make revenue when it processes wafers. It makes revenue when customers accept qualified wafers and products enter mass production.

8.1 Full customer value chain



Figure 5: Customer requirement-to-shipment flow, illustrating the progression from product definition and design through qualification, volume manufacturing, testing, packaging, and customer delivery.

8.2 Example: 28nm microcontroller (MCU) value chain



Figure 6: End-to-end 28 nm industrialization roadmap showing the transition from product definition to qualified mass production.

8.3 Typical timeline

Stage	Typical Duration
Product design	6-18 months
Tape-out and mask preparation	1-2 months
Wafer fabrication	2-4 months
Packaging and final test	2-6 weeks
Customer qualification	3-12 months
Production ramp	6-24 months

8.4 Customer requirements

A customer will require:

- Stable PDK
- Proven IP
- Qualified standard cells
- SRAM data
- SPICE models
- Stable design rules
- MPW shuttle capability
- Competitive cycle time
- Reliability reports
- Yield visibility
- Failure-analysis support
- Long-term supply assurance
- Change-control discipline
- Quality systems
- Customer engineering support

> ***Key message:***
>
> *A new foundry must sell more than wafer capacity. It must sell trust.*

9. Yield Economics

Yield is the difference between a technically impressive fab and a profitable fab. A fab can have following functionalities and still lose money if yield is poor:

- Excellent equipment
- A functioning cleanroom
- Strong process technology
- Large capacity

9.1 Yield flow

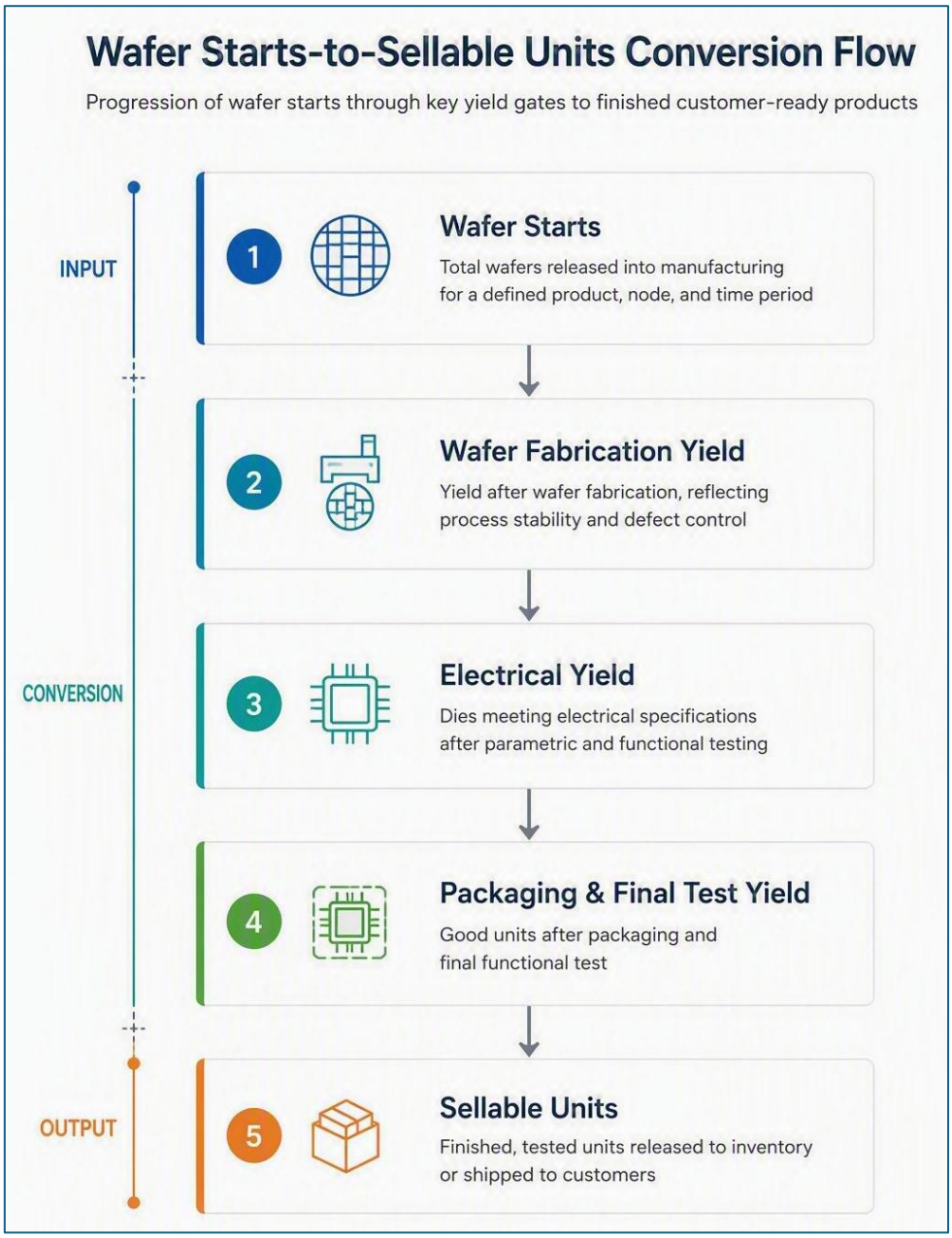


Figure 7: Simplified yield flow showing the conversion of wafer starts into sellable units through fabrication, electrical, packaging, and final-test yield gates.

Yield loss at any stage reduces the number of sellable products generated from the original wafer investment.

9.2 Cost per good die

$$Cost\ per\ good\ die = {Total\ processed\ wafer\ cost}/{Good\ dies\ per\ wafer}$$

To calculate good dies per wafer, start with the gross dies per wafer calculation:

$$Gross\ Dies/Wafer \approx \frac{\pi r^2}{A_{die}} - \frac{\pi D}{\sqrt{2A_{die}}}$$

where: r = wafer radius, D = wafer diameter, A_{die} = area of one die, πr^2 = total wafer area. First term $\frac{\pi r^2}{A_{die}}$ refers to the theoretical maximum, i.e., If the wafer were an infinitely large rectangular sheet, how many dies could its area theoretically contain? The second term $\frac{\pi D}{\sqrt{2A_{die}}}$ refers to the edge-loss correction, i.e., geometric correction for dies that cannot fit completely near the circular wafer edge.

For a 300mm wafer, the gross die calculation will give the following number, based on the die size:

Die Size	Approx. Gross Dies / Wafer
50 mm^2	~1,320
100 mm^2	~640
150 mm^2	~417

Good dies per wafer depend on:

- Die size
- Edge exclusion
- Defect density
- Process maturity
- Parametric yield
- Test yield
- Packaging yield

The economics become particularly sensitive as die size increases because larger dies are statistically more exposed to random defects.

A useful approximation is:

$$Good\ dies\ per\ wafer = Gross\ dies\ per\ wafer \times Functional\ yield$$

To calculate defect limited yield, A simple Poisson yield approximation can be used:

$$Yield = e^{(-D_0\ X\ A)}$$

Where, D_0 = defects/cm^2, A = die area in cm^2

Example for a 100mm^2 (=1 cm^2) die, assuming defect density to be in the range of 0.1 defects/cm^2.

$$Yield = e^{(-0.1 \times 1)} = 90.5\%$$

Good dies per wafer calculation (assuming following wafer sort and packaging yield):

Parameter	Value
Die size	100 mm²
Gross dies / wafer	640
Functional yield	90.5%
Wafer sort yield	98%
Packaging yield	99%

$$Good\ packaged\ units: 640 \times 90.5\% \times 98\% \times 99\% = \mathbf{562\ units}$$

Finally, to calculate the number of good units and final cost per good unit based on following assumptions:

- 100mm^2 die
- 640 gross dies/wafer
- Functional yield of 70% vs. 80%
- combined test + packaging yield = 97%
- wafer price or processed wafer cost = US$2,500

$$Good\ units = 640 \times 70\% \times 97 = 435$$

$$Cost\ per\ good\ unit = 2{,}500 \div 435$$

= *US$ 5.75*

$$Good\ units = 640 \times 80\% \times 97 = 497$$

$$Cost\ per\ good\ unit = 2500 \div 497$$

= *US$ 5.03*

This calculation shows that improving functional yield from 70% to 80% reduces cost per good unit by ~ 12.5%, which can be hugely beneficial for a manufacturing plant.

9.3 Sensitivity factors

Variable	Impact
Die size	Determines gross die count and defect sensitivity
Defect density	Determines functional yield
Wafer cost	Direct manufacturing input
Utilization	Spreads fixed costs
Depreciation	Major fixed-cost burden
Cycle time	Affects throughput and cash conversion
Scrap	Direct margin loss
Test yield	Reduces sellable units
Packaging yield	Affects final unit economic

A sustained improvement from 70% to 80% yield can have a major financial impact, but the actual value depends on wafer starts, die size, ASP, product mix and cost structure. This is why following are not simply engineering functions but are financial functions:

- Defect inspection
- Metrology
- Statistical process control (SPC)
- Advanced process control (APC)
- Faults detect and classification (FDC)
- Process integration
- Equipment stability

> ***Key message:***
>
> *Yield is the primary driver of semiconductor manufacturing economics. Every yield loss, from wafer fabrication through final test and packaging, reduces the number of sellable units and increases the cost per good die. As a result, functions such as defect inspection, metrology, SPC, APC, FDC, and equipment stability are not only engineering enablers but also critical drivers of profitability.*

10. Fab Economics and Profit and Loss (P&L) statement

10.1 CAPEX structure

The following ranges are indicative planning assumptions for a mature node 300mm fab. Actual project accounting varies significantly by country, subsidies, building design, equipment strategy, technology scope, and whether certain infrastructure is shared or pre-existing.

CAPEX item	Typical share
Process equipment	50–65%
Fab building and cleanroom	15–25%
Utilities and facilities	10–20%
Metrology and inspection	5–10%
Automation and IT	3–5%
Qualification and startup	3–8%

These categories can overlap depending on project accounting, so they should not automatically be summed as fixed industry percentages. The major CAPEX driver remains process equipment. And process-equipment CAPEX is determined by:

Technology → Process flow → Process steps → Wafer volume → Throughput → Redundancy → Tool count

Global 300mm equipment spending illustrates the scale of the manufacturing ecosystem. SEMI's published outlook has projected extremely high global spending on 300mm fab equipment through the latter part of the decade. [2] However, global equipment spending should not be confused with the CAPEX requirement of an individual fab.

10.2 OPEX structure

OPEX item	Main cost driver
Materials	Wafer starts, layer count, process complexity
Utilities	Power, water, gases, HVAC, abatement
Labor	Headcount, shift model, local wage level
Maintenance	Tool uptime, spare parts, service contracts
Depreciation	CAPEX and accounting life

Waste treatment	Chemical and slurry intensity
Logistics	Materials, masks, wafers and spare parts
Customer support	PDK, FA, quality and application engineering
IT / automation	MES, APC, FDC, data infrastructure

The critical distinction is between fixed and variable costs.

Major fixed or semi-fixed costs

- Depreciation
- Facilities
- Core engineering workforce
- Base utilities
- Maintenance infrastructure
- IT/MES
- Security
- EHS

More variable costs

- Process materials
- Consumables
- Some utilities
- Packaging
- Logistics
- Certain maintenance expenses

This creates one of the fundamental economic characteristics of semiconductor manufacturing:

Higher utilization spreads a large fixed-cost base across more good wafers.

10.3 Revenue formula

$$Annual\ Revenue = Installed\ WSPM \times Utilization \times 12 \times Blended\ ASP\ per\ wafer$$

This is a simplified revenue model. A full model must additionally consider:

- Product mix
- Yield
- Scrap
- Engineering wafers

- Customer discounts
- Mask/NRE revenue
- Different wafer ASPs
- Capacity reservation
- Packaging/test revenue, if included

10.4 Base-case revenue example

Parameter	Assumption
Installed capacity	40,000 WSPM
Utilization	85%
Effective wafers/year	408,000
Blended ASP	US$2,500/wafer
Annual revenue	~US$1.02B

Base case calculation:

$$Installed\ capacity = 40{,}000\ WSPM, Utilization = 85\%, Blended\ ASP = US\ 2{,}500/wafer$$

$$Annual\ wafers = 40{,}000\ \times 12\ \times 85\% = \mathbf{408{,}000\ wafers/year}$$

$$Annual\ Revenue = 408{,}000\ \times US\$\ 2{,}500 = \mathbf{US\ \$1.02B}$$

The US$1.02B figure is illustrative revenue, not projected profit. Actual profitability will depend on:

- Yield
- Product mix
- Wafer ASP
- Material cost
- Energy cost
- Labor
- Maintenance
- Depreciation
- Financing
- Taxes
- Customer-specific costs

10.5 Illustrative Profit & Loss Model

Base case: 45/40nm heavy mix

Item	Assumption
Annual wafers	408,000
Blended ASP	US$2,500
Revenue	US$1.02B
Variable cost / wafer	US$1,100
Variable cost	US$449M
Fixed cash OPEX	US$250M
EBITDA	US$321M

Calculation:

$$Variable\ cost = 408{,}000 \times US\ \$\,1{,}100 = US\ \$449M$$

$$EBIDTA = US\ \$1.02B - US\ \$449M - US\ \$250M = US\$321M$$

$$EBIDTA\ margin \approx 31.5\%$$

Important Depreciation Reality

If CAPEX is US$8B and depreciation is modelled over 10 years:

$$Annual\ depreciation = US\ \$8B\ \div 10 = US\$800\,M/year$$

Therefore,

$$EBIT = EBIDTA - deprecitaiton = \ \boldsymbol{-US\$479M}$$

The calculated value of −US$479 million per year illustrates the challenge of recovering the substantial capital investment required for semiconductor manufacturing. Although the fab may generate positive operating margins before depreciation, the annual cost of an US$8 billion investment can outweigh these earnings. Consequently, fab profitability is highly sensitive to utilization, yield, average selling price (ASP), product mix, depreciation assumptions, and

government support mechanisms. Achieving sustainable returns therefore requires not only technology leadership but also strong manufacturing execution and high-volume customer demand. This shows why fab economics are extremely sensitive to utilization, subsidies, depreciation life, customer ASP, and product mix.

10.6 Break-even Utilization

A 28nm/45nm fab does not have a universal break-even utilization level. The break-even point depends on:

- CAPEX
- Depreciation
- ASP
- Yield
- Variable cost per wafer
- Fixed OPEX
- Financing cost
- Product mix
- Subsidies
- Technology royalties

The relevant calculation is:

$$Breakeven\ wafers = Fixed\ cash\ OPEX/[(ASP - variable\ cost\ per\ wafer) \times annual\ installed\ capacity]$$

Base case:

$$Fixed\ cash\ OPEX = US\ \$250M, ASP = US\ \$2{,}500, Variable\ cost = US\$1{,}100, Installed\ annual\ capacity = 480{,}000\ wafer$$

$$Break\ even\ utilization = 250 \div [(2{,}500 - 1{,}100) \times 480{,}00] = 37.2\%$$

This is cash EBITDA break-even, excluding depreciation. Full capital recovery is much harder. If depreciation is included (assuming capex of US$8B for a depreciation period of 10years):

$$Fixed\ cost\ including\ depreciation = Fixed\ cash\ opex + Depreciation\ per\ year = US\$250M + US\$800M = US\$1.05B$$

$$Capital - recovery\ utilization = 1.05B \div 672M = \mathbf{156\%}$$

It means that under these assumptions, even operating the fab at 100% utilization would not generate enough EBITDA contribution to cover $800M annual depreciation plus $250M fixed cash OPEX. The fab theoretically would need to be operating at 150% utilization, which is not possible. This simply means that the base case cannot fully recover an US$8B investment at US$2,500/wafer and 40,000 WSPM unless one or more variables improve:

- higher ASP
- higher utilization
- higher capacity
- lower CAPEX
- subsidies
- longer depreciation life
- better product mix
- lower variable cost
- or capacity expansion

Strong Case: 28nm-heavy mix

Parameter	Assumption
Capacity	40,000 WSPM
Utilization	**90%**
Annual wafers	432,000
ASP	**US$3,000**
Revenue	US$1.296B
Variable cost / wafer	US$1,200
Variable cost	US$518M
Fixed cash OPEX	US$250M
EBITDA	**US$528M**

The 28 nm-heavy mix scenario assumes that a greater proportion of production is allocated to higher-value 28 nm products rather than lower-ASP mature-node devices. Although manufacturing capacity remains fixed at 40,000 WSPM, the higher-value product mix increases the average selling price from US$2,500 to US$3,000 per wafer, resulting in annual revenue of approximately US$1.3 billion and EBITDA of US$528 million. This illustrates that product mix can be just as important as utilization in determining fab profitability, as the same physical capacity can generate significantly different financial outcomes depending on the value of the products being manufactured.

Despite the stronger operating performance, recovering the underlying capital investment remains challenging. Assuming an US$8 billion fab depreciated over 10 years, annual depreciation is approximately US$800 million, which exceeds the US$528 million EBITDA generated in this scenario. As a result, the fab remains below full economic break-even, although the gap is substantially smaller than in the base-case scenario. This highlights the importance of moving toward higher-value products, improving yields, increasing utilization, securing government incentives, and optimizing the overall cost structure.

More broadly, there is no universal utilization threshold at which a semiconductor fab becomes profitable. Break-even utilization depends on a combination of factors, including capital intensity, depreciation assumptions, product mix, ASP, yield performance, government support, and operating costs. Consequently, statements such as "75% utilization is break-even" should be viewed as scenario-specific assumptions rather than industry-wide rules.

For the purpose of economic stress testing, the following utilization ranges provide a practical framework:

- 70% utilization: Downside case
- 80-85% utilization: Base case
- 90% utilization: Strong operating case

New fabs are particularly vulnerable during the ramp-up phase because many costs, including depreciation, facilities, engineering support, maintenance infrastructure, and core staffing, remain largely fixed regardless of output volume. As a result, even modest improvements in utilization can have a disproportionate impact on profitability by spreading fixed costs across a larger number of wafers and sellable units.

> ***Key message:***
>
> *Utilization drives cost absorption, but product mix drives value creation. Sustainable fab profitability requires both high utilization and a sufficient share of higher-value products to recover the multibillion-dollar capital investment.*

11. Supply Chain Risk

Supply-chain risk is one of the most underestimated parts of fab planning. A semiconductor fab depends on a globally interconnected ecosystem of:

- Equipment
- Components
- Materials
- Chemicals
- Gases
- Wafers
- Reticles
- Spare parts
- Software
- Process IP
- Field-service engineers

11.1 Supplier map

Area	Key global suppliers
Lithography	ASML, Nikon, Canon
Tracks	TEL, SCREEN
Etch	Lam Research, TEL, Applied Materials
Deposition	Applied Materials, Lam Research, TEL, ASM
CMP tools	Applied Materials, Ebara, Lam Research
Metrology and inspection	KLA, Applied Materials, Onto, Nova
Photoresist	JSR, TOK, Shin-Etsu, Fujifilm, Sumitomo
CMP materials	Entegris, Fujimi, DuPont, Resonac
Wafers	Shin-Etsu, SUMCO, GlobalWafers, Siltronic
Gases	Linde, Air Liquide, Air Products, Taiyo Nippon Sanso
Wet chemicals	BASF, Mitsubishi Chemical, Kanto, Honeywell, Solvay

The supplier list should not be interpreted as a complete approved-vendor list. Actual qualification depends on process, geography, quality requirements and technology platform.

11.2 Supply-chain risk index

A practical screening framework:

$$Risk\ Score = Supplier\ Concentration \times Geopolitical\ exposure \times Qualification\ difficulty \times Switching\ cost \times Lead\ time\ sensitivity$$

The score should then be expanded to include:

- Inventory coverage
- Alternate supplier availability
- Local manufacturing capability
- Logistics vulnerability
- Service dependency

11.3 Highest-risk areas

Item	Risk Level
Lithography tools	Very high
Advanced photoresists	High
High-purity wafers	High
Specialty gases	Medium-high
Metrology and inspection	High
Wet chemicals	Medium
CMP materials	Medium
Tool spare parts	High
Process IP	Very high

Key message:

A fab can be delayed not only by missing scanners, but also by missing spare parts, masks, process gases, qualified chemicals, or service engineers. Supply-chain resilience must therefore be designed into the fab from day one.

12. The Customer Problem

A fab does not exist because the technology is interesting. It exists because customers buy wafers.

12.1 Target markets for 28nm/45nm

Market	Fit for 45/28nm
Automotive	Strong
Industrial	Strong
Connectivity	Strong
Display	Strong
Consumer electronics	Medium-strong
IoT	Strong
RF/mixed signal	Selective
Edge AI	Selective
AI infrastructure	Limited for main compute, stronger for support chips

The key distinction is that 28nm should not be positioned as a replacement for leading-edge nodes in AI accelerators or high-performance CPUs. Its opportunity is stronger in supporting silicon and edge/embedded applications where power, cost, integration, longevity and supply assurance matter.

12.2 Demand equation



Figure 8: Market-to-fab conversion flow showing how total market opportunity narrows into qualified demand, committed wafers, and actual WSPM loading.

For a 40,000 WSPM fab at 85% utilization:

$$40{,}000 \times 85\% = 34{,}000 \ {}^{wafers}/_{month}$$

The investment committee question is simple:

> ***Key question:*** *Can the new fab realistically secure 34,000 wafers/month of qualified demand at acceptable pricing? If not, the fab will struggle financially even if the technology works.*

12.3 Customer acquisition strategy

A new fab should secure:

- 2–3 anchor customers.
- 5–10 medium-volume customers.
- Multi Project Wafer (MPW) shuttle program.
- Domestic or regional design-house pipeline.
- Long-term supply agreements.
- Automotive and industrial qualification roadmap.
- Customer engineering and FA support.

The customer pipeline should be measured in following rather than the number of customer logos:

$$\boldsymbol{WSPM \times ASP \times Qualification\ status \times Expected\ Ramp\ date}$$

> ***Key message:***
>
> *Customer trust is as important as process technology.*

13. Build vs Buy Strategic Options

A new manufacturer does not have only one path. The strategic route can materially change:

- CAPEX
- Technology risk
- Ramp time
- Workforce requirements
- Customer confidence
- Long-term control

Option	Advantages	Disadvantages	Time-to-Revenue
Greenfield fab	Full control, modern design, scalable	Highest CAPEX, longest ramp	4-7 years
Acquire existing fab	Faster entry, existing workforce	Legacy tools, limited scalability	1-3 years
Convert older fab	Lower CAPEX, faster start	May not support 300mm/28nm efficiently	2-4 years
JV with existing foundry	Lower technology risk	Shared control, partner dependence	2-5 years
Technology licensing	Faster process access	Royalty/IP dependence	2-5 years
Technology-transfer partnership	Reduces process risk	Requires partner alignment	2-5 years

Recommended strategy for a new entrant:

The most realistic path is:



Figure 9: Customer-led fab ramp strategy showing how committed demand, technology partnership, platform readiness, qualification, and yield stabilization enable lower-risk 28 nm expansion.

This approach reduces the risk of attempting technology development, fab construction, customer acquisition and yield ramp simultaneously. A pure independent greenfield 28nm fab is possible, but it carries significantly higher technology, operational, customer and financial risk.

14. Three Scenario Comparison

A new manufacturer should compare three strategies before committing capital

Metric	180/130nm Strategy	45/40nm Strategy	28nm Strategy
CAPEX	US$3B-5B	US$5B-8B	US$7B-10B
WSPM	40k	40k	40k
Base ASP / wafer	US$1,500	US$2,300	US$3,000
Revenue at 85% utilization	US$612M	US$938M	US$1.224B
Employees	~2,000	~2,700	~3,000
Technical difficulty	Low-medium	High	Very high
Yield-ramp difficulty	Low-medium	High	Very high
Equipment complexity	Medium	High	Very high
Materials complexity	Medium	High	Very high
Payback risk	Medium	Medium-high	High
Strategic value	Medium	High	Very high

Interpretation

A new semiconductor manufacturer must balance capital requirements, technical capability, market positioning, and long-term profitability when selecting its initial process node strategy. Although all three scenarios assume the same nominal capacity of 40,000 wafer starts per month (WSPM), their economic profiles differ substantially due to differences in ASP, process complexity, yield learning, and capital intensity.

180/130 nm Strategy

The 180/130 nm strategy represents the lowest-risk entry path. Capital requirements are comparatively modest, manufacturing processes are mature, equipment availability is generally better, and yield learning is faster. These nodes continue to serve industrial, power management, mixed-signal, analog, sensor, and certain automotive applications. However, lower ASPs limit revenue generation and reduce the ability to absorb fixed costs associated with a modern fab. As a result, while execution risk is lower, long-term differentiation and strategic competitiveness may be constrained.

45/40 nm Strategy

The 45/40 nm strategy offers a stronger balance between technical complexity and economic value creation. These nodes support a broad range of applications including automotive microcontrollers, industrial processors, display drivers, connectivity devices, and networking products. ASPs are significantly higher than at 180/130 nm while the technology remains more accessible than 28 nm. Consequently, 45/40 nm may represent an attractive compromise for

emerging manufacturing ecosystems seeking a combination of commercial viability, manageable technical risk, and strategic relevance.

28 nm Strategy

The 28 nm strategy offers the highest long-term strategic value but also requires the greatest investment and operational discipline. Success depends on advanced process integration, tighter process control, more sophisticated metrology, stronger yield management, and a mature ecosystem of customers, suppliers, IP providers, and design partners. While the higher ASPs can generate substantially greater revenue and improve capital recovery potential, the fab becomes more sensitive to yield loss, utilization shortfalls, qualification delays, and customer concentration. As a result, successful 28 nm manufacturing typically requires stronger anchor customers and a well-developed demand pipeline before large-scale investments can be justified.

Strategic Implications

The comparison suggests that higher technology nodes do not automatically guarantee superior economics. A poorly utilized 28 nm fab may generate lower returns than a highly utilized 45/40 nm facility with strong customer commitments and stable yields. Consequently, technology selection should be driven not only by technical ambition but also by realistic assessments of:

- Customer demand and qualification readiness
- Expected utilization levels
- Product ASP and product mix
- Yield ramp capability
- Availability of skilled workforce
- Equipment and ecosystem maturity
- Government incentives and capital support
- Long-term market differentiation

> ***Key message:***
>
> *180/130 nm minimizes execution risk, 45/40 nm provides the strongest balance between risk and reward, while 28 nm maximizes strategic value but requires significantly stronger customer demand, operational maturity, yield performance, and capital commitment to achieve sustainable returns.*

15. Final Recommendation

A 28nm/45nm fab can be profitable, but profitability does not come from the node itself. It comes from the interaction of five models:

Model	Required Capability
Technology model	Process flow, architecture, PDK, IP, reliability
Fab model	Cleanroom, tools, utilities, automation, materials
Operations model	People, capacity, cycle time, yield, uptime
Financial model	CAPEX, OPEX, ASP, depreciation, cash flow, IRR
Market model	Customers, TAM, wafer demand, competition

These five models must be internally consistent. A technically excellent fab with no customers will fail. A fully booked fab with poor yield will fail. A high-yield fab with excessive CAPEX can fail. A profitable product with unreliable supply can lose customers. And a technically mature process without a competitive PDK and customer ecosystem will struggle to attract designs.

Final KPI Dashboard

KPI	Target
Utilization	>85%
Functional yield	>85%
Critical tool availability	>90%
Defect density	0.05-0.15 defects/cm^2
Cycle time	<120 days
On-time delivery	>95%
Customer retention	>90%
Qualified demand	>34,000 wafers/month for 40k WSPM fab

The final answer to the original question is therefore:

Yes, a new manufacturer can build a profitable 28nm/45nm fab – but not by treating the fab as a construction project. It must be built as an integrated manufacturing business.

The winning sequence is:



Figure 10: End-to-end pathway showing how market demand, technology, fab capability, yield, and utilization translate into competitive cost and sustainable cash flow.

The ultimate objective is not to maximize wafer capacity. It is to maximize:

GOOD WAFERS × CUSTOMER VALUE × UTILIZATION × YIELD

while minimizing:

COST PER GOOD DIE × CAPITAL INTENSITY × OPERATIONAL RISK

That is what turns a semiconductor fab from an expensive industrial facility into a sustainable manufacturing business.

The final answer to the original question is:

> ***Yes, a new manufacturer can build a profitable 28nm/45nm fab, but not by treating the fab as a construction project. It must be built as an integrated manufacturing business with phased technology ramp, reliable supply chain, qualified customers, high utilization, and relentless yield discipline.***

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